CLAIMS

1. In a floating-point processor, an addition pipeline, adapted for application thereto of first and second operand signals, each of which represents the sign, exponent, and mantissa of a respective floating-point input operand, for performing an effective addition or subtraction on the input operands and generating an addition-pipeline ouput signal representing the result, the addition pipeline comprising:

A) a main mantissa adder adapted for application thereto of first and second processed mantissa signals and representing respective mantissa values, the main mantissa adder being operable selectively to perform addition and subtraction on the mantissa values and generate a mantissa-adder output, representative thereof, from which the addition pipeline generates the addition-pipeline ouput; and

B) mantissa-processing circuitry for so generating from respective ones of the input operands' mantissas and applying to the main mantissa adder respective processed mantissa signals that, for at least some pairs of mantissas, the mantissa signals applied to the main mantissa adder when the main mantissa adder is to subtract a pair of mantissas are offset to the left by one position from the mantissa signals applied thereto when the main mantissa adder is to add the same pair of mantissas.

2. An addition pipeline as defined in claim 1 wherein the main mantissa adder performs a nomalization shift when necessary to produce an output within predetermined normalization limits but is capable of performing the normalization shift in only one direction..

3. An addition pipeline as defined in claim 2 wherein the main mantissa adder is capable of performing the normalization shift only to the right.

4. An addition pipeline as defined in claim 2 wherein the mantissa-processing circuitry comprises a pair of processing trains for generating first and second processed mantissa signals from respective input operands' mantissas, each processing train performing a shift, for at least a plurality of input-operand-value pairs, that is one more position to the left for an effective subtraction than for an effective addition.

5. An addition pipeline as defined in claim 2 wherein the main mantissa adder includes rounding circuitry operable in at least one rounding mode to add a rounding bit and being capable of adding the rounding bit at a selected one of only two bit positions in a given rounding mode.

6. An addition pipeline as defined in claim 1 wherein the main mantissa adder includes rounding circuitry operable in at least one rounding mode to add a rounding bit and being capable of adding the rounding bit at a selected one of only two bit positions in a given rounding mode.

7. An addition pipeline as defined in claim 1 wherein the mantissa-processing circuitry comprises a pair of processing trains for generating first and second processed mantissa signals from respective input operands' mantissas, each processing train performing a shift, for at least a plurality of input-operand-value pairs, that is one more position to the left for an effective subtraction than for an effective addition.